# 2.7 V to 5.25 V, Micro Power, 8-Channel, 200 kSPS, 12-Bit ADC in 16-Pin TSSOP

## Preliminary Technical Data — AD7888

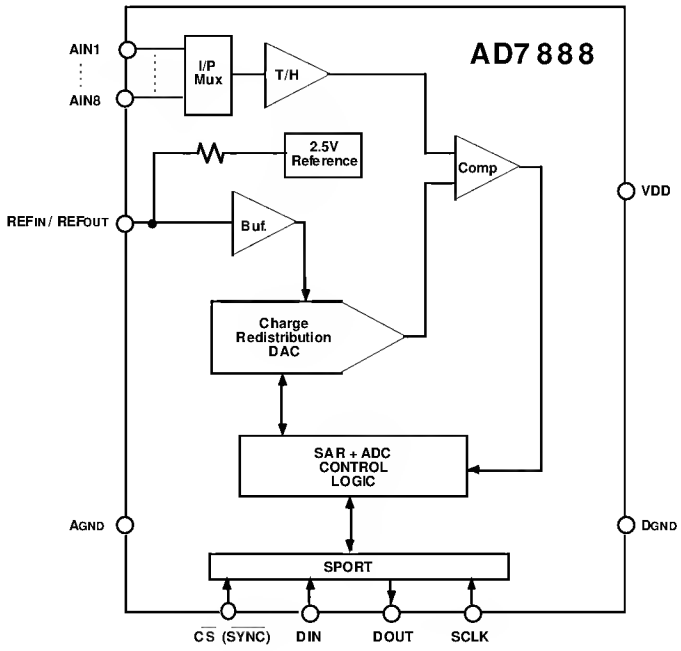
### FEATURES

**Specified for $V_{DD}$ of 2.7 V to 5.25 V**
**700 μA max @ 200 kSPS Throughput.**
**450 μA max @ 100 kSPS Throughput**
**Shut Down Mode 1μA max**
**Eight Single-Ended Inputs**
**Serial Interface: SPI/QSPI/μWire**
**16-Pin Narrow SOIC and TSSOP Packages**

### APPLICATIONS

**Battery-Powered Systems (Personal Digital Assistants, Medical Instruments, Mobile Communications)**
**Instrumentation and Control Systems**
**High Speed Modems**

### FUNCTIONAL BLOCK DIAGRAM




### GENERAL DESCRIPTION

The AD7888 is a high speed, low power, 12-bit ADC that operate from a single 2.7 V or 5.25 V power supply. The AD7888 is capable of 200 kHz throughput rate. The input track-and-hold acquires a signal in 500 ns and features a single ended sampling scheme. The AD7888 voltage range is 0 to $V_{REF}$ with straight binary output coding. Input signal range is to the supply and the part is capable of converting full power signals to 3MHz.

CMOS construction ensures low power dissipation of typically 2 mW for normal operation and 3 μW in power-down mode. The part is available in a 16-lead narrow body small outline (SOIC) and a 16-lead thin small shrink outline (TSSOP) package.

### PRODUCT HIGHLIGHTS

1. Smallest 12-Bit 8-Channel ADC; 16-pin TSSOP is the same area as an 8-pin SOIC and less than half the height.
2. Lowest Power 12-Bit 8-channel ADC.
3. Flexible power management options including automatic powerdown after conversion.
4. Analog input range from 0 V to $V_{REF}$.
5. Versatile serial I/O port (SPI/QSPI/μWire).

Prelim A3. 2/97



**One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.**
**Tel: 617/329-4700** **Fax: 617/326-8703**

# AD7888–SPECIFICATIONS[1]

**($V_{DD}$ = +2.7 V to +5.25 V, $REF_{IN}/REF_{OUT}$ = 2.5 V External/Internal Reference unless otherwise noted, $f_{SCLK}$ = 3.2 MHz; $f_{SAMPLE}$ = 200 kHz; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)**

| Parameter | A Version[1] | B Version[1] | Units | Test Conditions/Comments |
|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | |
| Signal to Noise + Distortion Ratio[2] (SNR) | 70 | 71 | dB min | Typically SNR is 72 dB<br>$V_{IN}$ = 10 kHz Sine Wave, $f_{SAMPLE}$ = 200 kHz |
| Total Harmonic Distortion (THD) | –78 | –78 | dB max | $V_{IN}$ = 10 kHz Sine Wave, $f_{SAMPLE}$ = 200 kHz |
| Peak Harmonic or Spurious Noise | –78 | –78 | dB max | $V_{IN}$ = 10 kHz Sine Wave, $f_{SAMPLE}$ = 200 kHz |
| Intermodulation Distortion (IMD) | | | | |
| Second Order Terms | –78 | –80 | dB typ | fa = 9.983 kHz, fb = 10.05 kHz, $f_{SAMPLE}$ = 200 kHz |
| Third Order Terms | –78 | –80 | dB typ | fa = 9.983 kHz, fb = 10.05 kHz, $f_{SAMPLE}$ = 200 kHz |
| Channel-to-Channel Isolation | –90 | –90 | dB typ | $V_{IN}$ = 25 kHz |
| Full Power Bandwidth | | | MHz typ | @ 3 dB |
| DC ACCURACY | | | | Any Channel |
| Resolution | 12 | 12 | Bits | |
| Integral Nonlinearity | ±2 | ±1 | LSB max | |
| Differential Nonlinearity | ±1 | ±1 | LSB max | Guaranteed No Missed Codes to 12 Bits. |
| Total Unadjusted Error | ±3 | ±3 | LSB typ | |
| Unipolar Offset Error | ±3 | ±3 | LSB max | |
| Unipolar Offset Error Match | 3 | 3 | LSB max | |
| Positive Full-Scale Error | ±3 | ±3 | LSB max | |
| Positive Full-Scale Error Match | 3 | 3 | LSB max | |
| ANALOG INPUT | | | | |
| Input Voltage Ranges | 0 to $V_{REF}$ | 0 to $V_{REF}$ | Volts | |
| Leakage Current | ±1 | ±1 | µA max | |
| Input Capacitance | 20 | 20 | pF typ | |
| REFERENCE INPUT/OUTPUT | | | | |
| $REF_{IN}$ Input Voltage Range | 2.3/$V_{DD}$ | 2.3/$V_{DD}$ | V min/max | Functional from 1.2 V |
| Input Impedance | 10 | 10 | kΩ typ | |
| $REF_{OUT}$ Output Voltage | 2.475/2.525 | 2.475/2.525 | V min/max | |
| $REF_{OUT}$ Tempco | 20 | 20 | ppm/°C typ | |
| LOGIC INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | 2.4 | 2.4 | V min | $V_{DD}$ = 4.75 V to 5.25 V |
| | 2.1 | 2.1 | V min | $V_{DD}$ =2.7 V to 3.6V |
| Input Low Voltage, $V_{INL}$ | 0.8 | 0.8 | V max | $V_{DD}$ = 2.7 V to 5.25 V |
| Input Current, $I_{IN}$ | ±10 | ±10 | µA max | Typically 10 nA, $V_{IN}$ = 0 V or $V_{DD}$ |
| Input Capacitance, $C_{IN}$[3] | 10 | 10 | pF max | |
| LOGIC OUTPUTS | | | | |
| Output High Voltage, $V_{OH}$ | | | | $I_{SOURCE}$ = 400 µA |
| | $V_{DD}$ -0.5 | $V_{DD}$ -0.5 | V min | $V_{DD}$ = 2.7 V to 5.25 V |
| Output Low Voltage, $V_{OL}$ | 0.4 | 0.4 | V max | $I_{SINK}$ =1.6 mA |
| Floating-State Leakage Current | ±10 | ±10 | µA max | |
| Floating-State Output Capacitance[4] | 10 | 10 | pF max | |
| Output Coding | Straight (Natural) Binary | | | |
| CONVERSION RATE | | | | |
| Throughput Time | 16 | 16 | SCLK cycles | Conversion Time + Acquisition Time |
| Track/Hold Acquisition Time | 1.5 | 1.5 | SCLK cycles | |
| Conversion Time | 14.5 | 14.5 | SCLK cycles | |

| Parameter | A Version[1] | B Version[1] | Units | Test Conditions/Comments |
|---|---|---|---|---|
| POWER REQUIREMENTS | | | | |
| $V_{DD}$ | +2.7/+5.25 | +2.7/+5.25 | V min/max | |
| $I_{DD}$ | | | | |
| Normal Mode[4] | 700 | 700 | µA max | $f_{SAMPLE}$ = 200 kHz |
| Using Standby Mode | 450 | 450 | µA max | $f_{SAMPLE}$ = 100 kHz |
| Using Shutdown Mode | 50 | 50 | µA max | $f_{SAMPLE}$ = 10 kHz |
| Using Shutdown Mode | 6 | 6 | µA max | $f_{SAMPLE}$ = 1 kHz |
| Standby Mode | 200 | 200 | µA max | $V_{DD}$ = 4.75 V to 5.25 V. Typically 150 nA |
| Shutdown Mode | 1.0 | 1.0 | µA max | $V_{DD}$ = 4.75 V to 5.25 V. Typically nA |
| Normal Mode Power Dissipation | 3.675 | 3.675 | mW max | $V_{DD}$ = 5.25 V. Typically mW |
| | 2.1 | 2.1 | mW max | $V_{DD}$ = 3.0 V. Typically mW |
| Shutdown Power Dissipation | | | µW typ | $V_{DD}$ = 5.25 V. |
| | | | µW typ | $V_{DD}$ = 3.0 V. |
| Standby Power Dissipation | | | µW typ | $V_{DD}$ = 5.25 V. |
| | | | µW typ | $V_{DD}$ = 3.0 V. |

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2]SNR calculation includes distortion and noise components.
[3]Sample tested @ +25°C to ensure compliance.
[4]All digital inputs @ DGND except $\overline{SYNC}$ @ $V_{DD}$. No load on the digital outputs. Analog inputs @ AGND.
[5]SCLK @ DGND when SCLK off. All digital inputs @ DGND except for $\overline{SYNC}$ @ $V_{DD}$. No load on the digital outputs. Analog inputs @ AGND.
Specifications subject to change without notice.

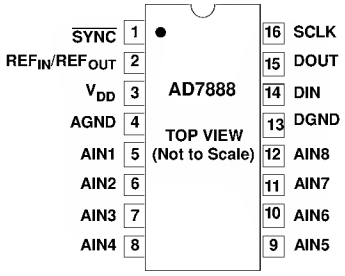
## ABSOLUTE MAXIMUM RATINGS[1]

($T_A$ = +25°C unless otherwise noted)

$V_{DD}$ to AGND ..... –0.3 V to +7 V
$V_{DD}$ to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND ..... –0.3 V to $V_{DD}$ + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to $V_{DD}$ + 0.3 V
Digital Output Voltage to DGND ..... –0.3 V to $V_{DD}$ + 0.3 V
$REF_{IN}/REF_{OUT}$ to AGND ..... –0.3 V to $V_{DD}$ + 0.3 V
Input Current to Any Pin Except Supplies[2] ..... ±10 mA
Operating Temperature Range
Commercial (A, B Versions) .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Junction Temperature ..... +150°C
µSOIC, TSSOP Package, Power Dissipation .....450 mW
$\theta_{JA}$ Thermal Impedance . 75°C/W (µSOIC) 115°C/W (TSSOP)
$\theta_{JC}$ Thermal Impedance . .25°C/W (µSOIC) 35°C/W (TSSOP)
Lead Temperature, Soldering
Vapor Phase (60 secs) ..... +215°C
Infared (15 secs) ..... +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

## PINOUTS FOR SOIC AND TSSOP



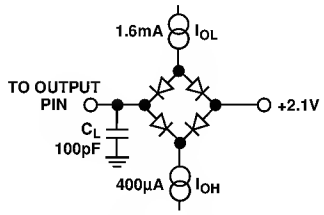




*Figure 1. Load Circuit for Digital Output Timing Specifications*

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## TIMING SPECIFICATIONS[1] ( $AV_{DD}$ = $DV_{DD}$ = +2.7 V to +5.25 V; $f_{SCLK}$ = 3.2 MHz ; $T_A$ = $T_{MIN}$ to $T_{MAX}$ , unless otherwise noted)

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ (A, B Versions) 5V | 2.7V | Units | Description |
|---|---|---|---|---|
| $f_{SCLK}$ | 3.2 | 3.2 | MHz max | |
| $t_{CONVERT}$ | 14 $t_{SCLK}$ | 14 $t_{SCLK}$ | | Throughput Time = $t_{CONVERT}$ + $t_{acq}$ = 16 $t_{SCLK}$ |
| $t_{acq}$ | 1.5 $t_{SCLK}$ min | 1.5 $t_{SCLK}$ min | | Throughput Time = $t_{CONVERT}$ + $t_{acq}$ = 16 $t_{SCLK}$ |
| $t_1$ | –0.4 $t_{SCLK}$ | –0.4 $t_{SCLK}$ | ns min | $\overline{SYNC}$↓ to SCLK↓ Setup Time (Noncontinuous SCLK Input) |
| | 70.4 $t_{SCLK}$ | 70.4 $t_{SCLK}$ | ns min/max | $\overline{SYNC}$↓ to SCLK↓ Setup Time (Continuous SCLK Input) |
| $t_2$[4] | 50 | 90 | ns max | Delay from $\overline{SYNC}$↓ Until DOUT 3-State Disabled |
| $t_3$[4] | | | ns max | Delay from $\overline{SYNC}$↓ Until DIN 3-State Disabled |
| $t_4$[4] | 75 | 115 | ns max | Data Access Time After SCLK↓ |
| $t_5$ | 40 | 60 | ns min | Data Setup Time Prior to SCLK↑ |
| $t_6$ | 20 | 30 | ns min | Data Valid to SCLK Hold Time |
| $t_7$ | 0.4 $t_{SCLK}$ | 0.4 $t_{SCLK}$ | ns min | SCLK High Pulse Width |
| $t_8$ | 0.4 $t_{SCLK}$ | 0.4 $t_{SCLK}$ | ns min | SCLK Low Pulse Width |
| $t_9$ | 30 | 50 | ns min | SCLK↑ to $\overline{SYNC}$↑ Hold Time (Continuous SCLK) |
| $t_{10}$[5] | 50 | 50 | ns max | Delay from $\overline{SYNC}$↑ Until DOUT 3-State Enabled |

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of $V_{DD}$) and timed from a voltage level of 1.6 Volts.

[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[3]The $\overline{SYNC}$ pulse width will here only applies for normal operation. When the part is in power-down mode, a different $\overline{SYNC}$ pulse width will apply (see Power-Down section).

[4]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[5]$t_{12}$ is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapo -lated back to remove the effects of charging or discharging the 100 pF capaci -tor. This means that the time, $t_{12}$, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

[6] $t_{14}$ is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the Timing Characteristics is the true delay of the part in turning off the output drivers and configuring the DIN line as an input. Once this time has elapsed the user can drive the DIN line knowing that a bus conflict will not occur.

Specifications subject to change without notice.

### ORDERING GUIDE

| Model | Linearity Error (LSB)[1] | Package Option[2] |
|---|---|---|
| AD7888AR | ±2 | R-16 |
| AD7888BR | ±1 | R-16 |
| AD7888ARU | ±2 | RU-16 |
| EVAL-AD7888CB[3] | | |
| EVAL-CONTROL BOARD[4] | | |

NOTES

[1]Linearity error here refers to integral linearity error.

[2]R = SOIC; RS = SSOP.

[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.

[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

## TYPICAL TIMING DIAGRAMS

Figures 2 shows the typical read and write timing diagrams for serial Interface of the AD7888. The reading and writing occurs during conversion.

The rising edge of the SCLK signal after the first one and one-half cycles ($t_{acq}$) of the SCLK, following the falling edge of the $\overline{SYNC}$ signal initiates the conversion on the AD7888.On the falling edge of $\overline{SYNC}$ line, the on-chip track/hold acquires the input signal for the first one and one-half cycles ($t_{acq}$) of the SCLK. On the next rising edge of the SCLK, the on-chip track/hold goes from track to hold mode.

The conversion cycle will take 14.5 SCLK periods from this SCLK rising edge. After the rising edge of the 16th SCLK edge, the conversion is complete, resulting in a conversion time of 5 µs ($16t_{SCLK}$, SCLK = 3.2 MHz). The $\overline{SYNC}$ input will then have to be taken high. If the $\overline{SYNC}$ is left low a new conversion will be initiated. The result of the conversion can be read by accessing the data through the serial interface during the conversion.

At least one and one-half periods of SCLK (acquisition time ) must be allowed (the time from the falling edge of SYNC to the next rising edge of $\overline{SCLK}$) before the next conversion begins to ensure that the part is settled to the 12-bit level.

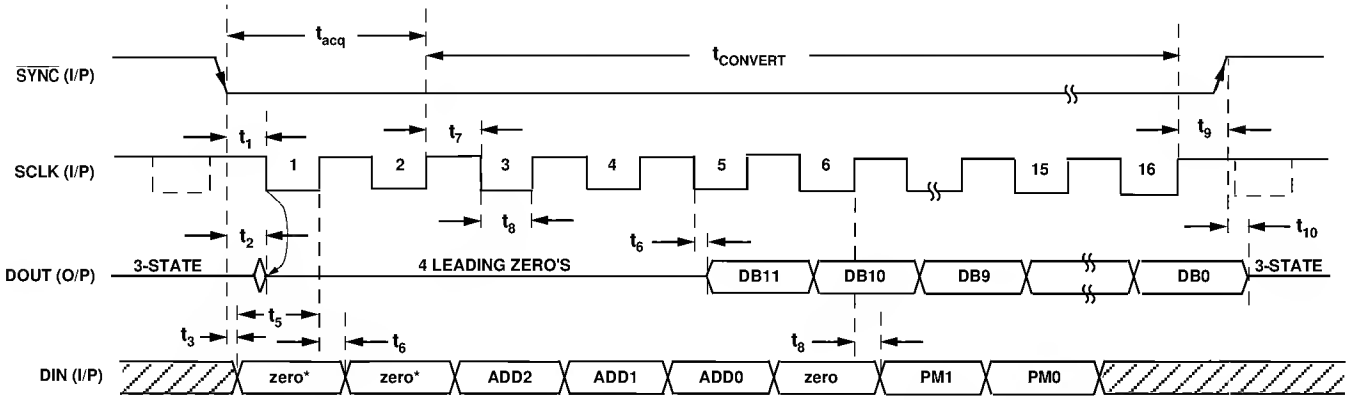



*Figure 2. AD7888 Timing Diagram for Reading/Writing during Conversion)*

**Table I. Power Management Options**

| PM1 Bit | PM0 Bit | Comment |
|---|---|---|
| 0 | 0 | **Normal Operation** |
| 0 | 1 | **Full Shutdown** |
| 1 | 0 | **Auto Shutdown** |
| 1 | 1 | **Standby** |

The AD7888 provides a number of power-down options. The four modes of operation are the Normal, Full Shutdown, Auto Shutdown and Standby. These options are controlled by the PM1 and PM0 bits in the Control Register. When both these bits are 0 (default status on power-up), the AD7888 is in normal mode of operation. With these bits at 0, 1 the part enters a Full Shutdown mode. With these bits at 1, 0 the AD7888 enters Full Shutdown mode after every conversion. Finally, with these bits at 1, 1 the part enters the Standby mode. The advantage of the Standby mode is that the part will require significantly less time to "power-up" than from the Full Shutdown mode. In this Standby mode the reference voltage stays powered up so if this is being used external to the AD7888 it is still available even though the AD7888 is effectively powered down. Table I summaries the power management options.

**Table II. Address Decode Options**

| ADD2 Bit | ADD1 Bit | ADD0 Bit | Comment |
|---|---|---|---|
| 0 | 0 | 0 | **Ain 1** |
| 0 | 0 | 1 | **Ain 2** |
| 0 | 1 | 0 | **Ain 3** |
| 0 | 1 | 1 | **Ain 4** |
| 1 | 0 | 0 | **Ain 5** |
| 1 | 0 | 1 | **Ain 6** |
| 1 | 1 | 0 | **Ain 7** |
| 1 | 1 | 1 | **Ain 8** |